Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Previously Presented) A magnetic random access memory device, comprising:

an array of magnetic elements;

a plurality of conductive lines configured to set magnetization states of the magnetic elements; and

circuitry configured to independently vary aspects of current applications along one or more of the conductive lines, wherein the aspects comprise at least one of:

an amount of current applied to the one or more conductive lines;

a point in time at which current is applied to the one or more conductive lines; and

a length of time current is applied to the one or more conductive lines.

2. (Canceled)

3. (Previously Presented) The magnetic random access memory device of claim 1, wherein the circuitry is configured to vary the amount of current with respect to the direction along which the current is applied.

4. (Previously Presented) The magnetic random access memory device of claim 1, wherein the circuitry is configured to vary the amount of current with respect to the temperature of the magnetic random access memory device.

5. - 6. (Canceled)

7. (Previously Presented) The magnetic random access memory device of claim 1, wherein the circuitry is configured to apply a write pulse current along one or more of the conductive lines for a length of time sufficient to allow a source current to be measured from a voltage power supply coupled to the magnetic random access memory device during the application of the write pulse current.

8. (Original) The magnetic random access memory device of claim 1, wherein the circuitry is configured to vary current applications for write operations of the magnetic random access memory device.

9. (Original) The magnetic random access memory device of claim 1, wherein the circuitry is configured to vary current applications for read operations of the magnetic random access memory device.

10. (Previously Presented) The magnetic random access memory device of claim 9, wherein the circuitry is further configured to vary an amount of bias voltage applied along a different conductive line comprising a gate of a transistor coupled to one of the magnetic elements.

11. (Previously Presented) The magnetic random access memory device of claim 1, wherein the circuitry is further configured to terminate the current applications upon determining a power level supplied to the magnetic random access memory device is below a predetermined threshold.

12. (Previously Presented) The magnetic random access memory device of claim 1, further comprising a reprogrammable non-volatile latch which is distinct from the array of magnetic elements and configured to store parameter settings for the current applications.

13. (Currently Amended) A device, comprising:

a magnetic random access memory (MRAM) array; and

a first storage circuit distinct from the MRAM array, wherein the first storage circuit comprises ~~and comprising~~ one or more magnetic elements, and wherein the first storage circuit is configured to store, within the magnetic elements, parameter

settings characterizing applications of current to operate the magnetic random access memory array.

14. (Original) The device of claim 13, wherein the parameter settings are settings selected for use by a customer of the device.

15. (Original) The device of claim 13, wherein the parameter settings are settings selected for testing qualitative features of the magnetic random access memory array.

16. (Previously Presented) The device of claim 13, further comprising an alternative means by which to store parameter settings characterizing applications of current to operate the magnetic random access memory array.

17. (Original) The device of claim 16, further comprising a second storage circuit having one or more magnetic elements, wherein the second storage circuit is configured to send a control signal by which to select the first storage circuit or the alternative means to send the parameter settings to the magnetic random access memory array.

18. (Original) The device of claim 13, further comprising circuitry configured to vary one or more values of the parameter settings during an operation of the magnetic random access memory array.

19. (Original) A magnetic random access memory device, comprising:

an array of magnetic elements;

a plurality of conductive lines configured to set magnetization states of the magnetic elements; and

circuitry configured to terminate an application of current along one or more of the conductive lines before magnetization states of one or more magnetic elements selected for a write operation of the device are changed.

20. (Original) The magnetic random access memory device of claim 19, wherein the circuitry is configured to:

monitor a voltage level of a power supply coupled to the magnetic random access memory device; and

terminate the application of current upon determining the voltage level is below a predetermined threshold.

21. (Original) A method, comprising:

coupling a power source to a magnetic random access memory device;

writing to at least one magnetic memory cell junction within the magnetic random access memory device;

monitoring current levels supplied from the power source; and

determining a write pulse amplitude for the magnetic junction based on a difference between a current level measured during the step of writing and a current level measured not during the step of writing.

22. (Original) The method of claim 21, wherein the step of determining a write pulse amplitude for the magnetic junction comprises determining a difference between the current level measured during the step of writing and a current level measured prior to the step of writing.

23. (Original) The method of claim 21, wherein the step of determining a write pulse amplitude for the magnetic junction comprises determining a difference between the current level measured during the step of writing and a current level measured subsequent to the step of writing.

24. (Original) The method of claim 21, wherein the step of writing comprises:

raising a voltage application along an address path of the magnetic random access memory device to a level higher than a voltage of the power supply; and

applying a current along a bit line coupled to the magnetic element for more than approximately 50 ns.

25. (Original) A method, comprising:

applying an initial bias voltage on a magnetic element of a memory cell array;

altering the bias voltage incrementally;

monitoring current levels associated with the initial bias voltage and the incremental bias voltages;

determining a difference in current levels between the initial bias voltage and an incremental bias voltage associated with a level of current corresponding to a midpoint between two logic states of the magnetic element; and

classifying the magnetic element as unsatisfactory upon determining the difference is less than a predetermined level.

26. (Original) The method of claim 25, wherein the step of altering the bias voltage incrementally comprises increasing the bias voltage.

27. (Original) The method of claim 25, wherein the step of altering the bias voltage incrementally comprises decreasing the bias voltage.